TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

SSM5N16FE

High Speed Switching Applications Analog Switching Applications

- Suitable for high-density mounting due to compact package
- Low on resistance: $R_{on} = 3.0 \Omega \text{ (max) } (@V_{GS} = 4 \text{ V})$

: $R_{on} = 4.0 \Omega \text{ (max) } (@V_{GS} = 2.5 \text{ V})$

: $R_{on} = 15 \Omega (max) (@V_{GS} = 1.5 V)$

Absolute Maximum Ratings (Ta = 25°C) (Q1, Q2 Common)

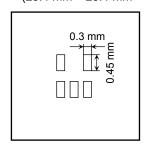
Characteristics		Symbol	Rating	Unit	
Drain-Source voltage		V_{DS}	20	V	
Gate-Source voltage		V _{GSS}	±10	V	
Drain current	DC	I _D	100	mA	
	Pulse	I _{DP}	200		
Drain power dissipation (Ta = 25°C)		P _D (Note 1)	150	mW	
Channel temperature		T _{ch}	150	°C	
Storage temperature range		T _{stg}	-55~150	°C	

Note:

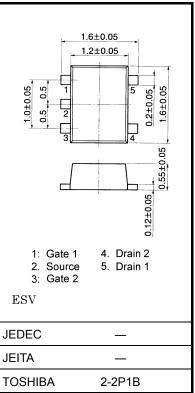
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Total rating, mounted on FR4 board (25.4 mm \times 25.4 mm \times 1.6 t, Cu Pad: 0.135 mm² \times 5)



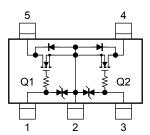
Unit: mm



Marking

5 4 D S D S

Equivalent Circuit



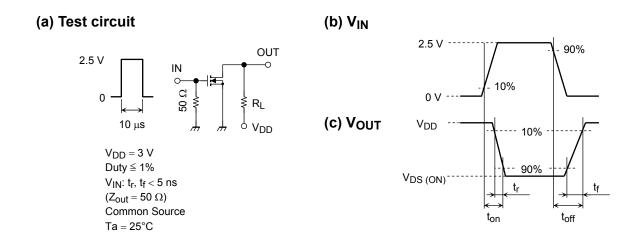
Handling Precaution

When handling individual devices (which are not yet mounting on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Electrical Characteristics (Ta = 25°C) (Q1, Q2 Common)

Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current		I _{GSS}	$V_{GS} = \pm 10 \text{ V}, V_{DS} = 0$	_	_	±1	μА
Drain-Source breakdown voltage		V (BR) DSS	$I_D = 0.1 \text{ mA}, V_{GS} = 0$	20	_	_	V
Drain cut-off curre	ent	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0	_	_	1	μА
Gate threshold vo	Itage	V _{th}	V _{DS} = 3 V, I _D = 0.1 mA	0.6	_	1.1	V
Forward transfer a	admittance	Y _{fs}	V _{DS} = 3 V, I _D = 10 mA	40	_	_	mS
Drain-Source ON resistance		R _{DS} (ON)	I _D = 10 mA, V _{GS} = 4 V	_	1.5	3.0	Ω
			I _D = 10 mA, V _{GS} = 2.5 V	_	2.2	4.0	
			I _D = 1 mA, V _{GS} = 1.5 V	_	5.2	15	
Input capacitance		C _{iss}	V _{DS} = 3 V, V _{GS} = 0, f = 1 MHz	_	9.3	_	pF
Reverse transfer capacitance		C _{rss}	V _{DS} = 3 V, V _{GS} = 0, f = 1 MHz	_	4.5	_	pF
Output capacitance		Coss	V _{DS} = 3 V, V _{GS} = 0, f = 1 MHz	_	9.8	_	pF
Switching time	Turn-on time	t _{on}	$V_{DD} = 3 \text{ V}, I_D = 10 \text{ mA}, V_{GS} = 0~2.5 \text{ V}$	_	70	_	ns
	Turn-off time	t _{off}			125		

Switching Time Test Circuit



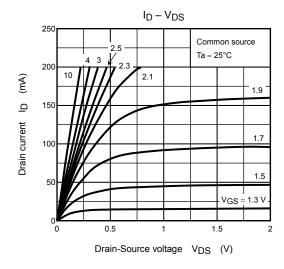
Precaution

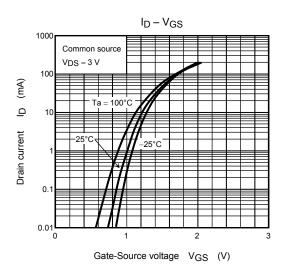
 V_{th} can be expressed as voltage between gate and source when low operating current value is I_D = 100 μA for this product. For normal switching operation, V_{GS} (on) requires higher voltage than V_{th} and V_{GS} (off) requires lower voltage than V_{th} . (Relationship can be established as follows: V_{GS} (off) < V_{th} < V_{GS} (on))

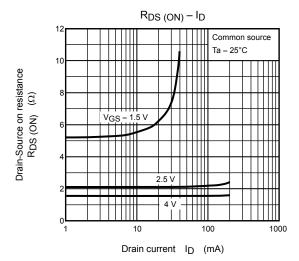
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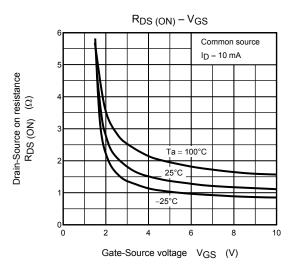
Please take this into consideration for using the device.

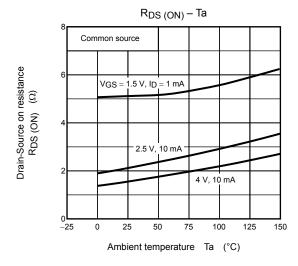
(Q1, Q2 common)

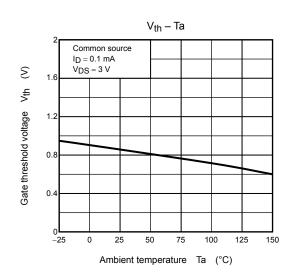




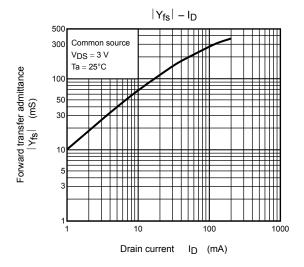


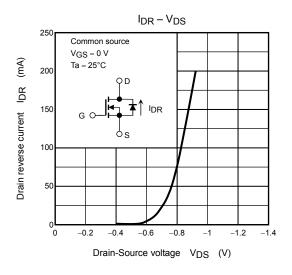


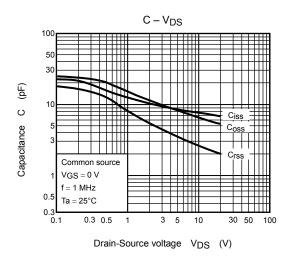


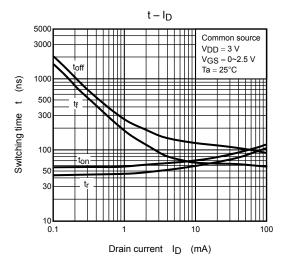


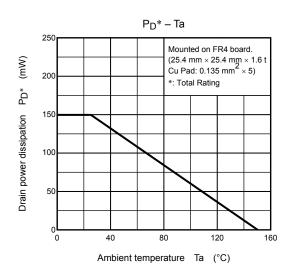
(Q1, Q2 common)











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20070701-EN GENERAL

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